Wide-Band Monolithic Phase Shifter

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Abstract—A wide-band monolithic phase shifter operating in the 2–8-GHz frequency range is described. Six GaAs FET's per bit are used as switch elements in a bridge configuration which alternatively becomes a high-pass or a low-pass section. Their low-impedance state is modeled as a resistor, the high-impedance state as a combination of capacitors and resistors. In the design approach, the high-impedance state equivalent shunt capacitor is not resonated. Instead, these capacitors become part of the resulting high-pass, low-pass sections. In this way, the maximum theoretical bandwidth that a high-pass, low-pass section can provide is achieved despite the nonideal switching elements.

I. Introduction

A LOW-PASS FILTER made up of series inductors and shunt capacitors provides phase delay to signals passing through it. A high-pass filter composed of series capacitors and shunt inductors provides phase advance. By arranging switch elements as shown in Fig. 1, to permit switching between low-pass and high-pass sections, it is possible to realize a compact phase shifter with wide-band performance [1]. The actual size and bandwidth of the phase shifter will also depend on the size and the low insertion, high-isolation bandwidth of the two 1×2 switches required for each phase bit.

For monolithic circuit applications, the available switch elements are FET's [2]–[5]. Unlike the p-i-n diode, the total capacitor shunting the high-impedance switch state is large; to realize the switching action, this capacitance must either be resonated or its effect must somehow be included in the design of the impedance-matching sections. In both cases, the bandwidth is limited.

A better approach would be to eliminate the input and output 1×2 switches completely; if this can be done, then one may expect to achieve the intrinsic bandwidth of the high-pass, low-pass sections alone. In addition, the savings in chip area will be quite significant, as the switches usually take more space than the phase-shifting sections.

This paper describes one such approach to achieving a wide-band phase-shifter function in monolithic form.

II. Design Considerations

Consider the circuit shown in Fig. 2. In this circuit, there are six discrete FET's, connected in two sets of T-configurations. The series elements of one T and the shunt element of the other T are switched from a single gate control voltage.

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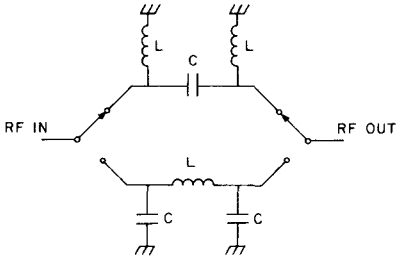

Fig. 1. A typical low-pass high-pass phase-shifter schematic circuit diagram.

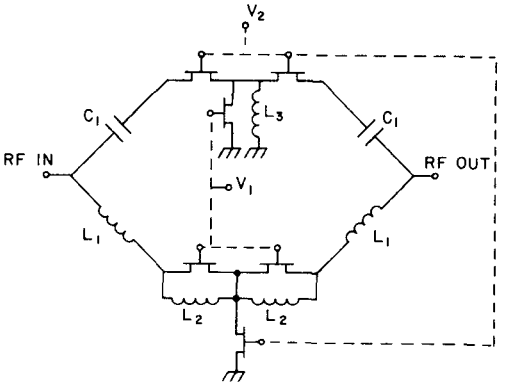

Fig. 2. Schematic circuit diagram for a single-bit phase shifter illustrating the present approach.

When the control voltage V_1 is zero and V_2 is beyond the pinchoff voltage V_p of the switch FET's, the circuit of Fig. 2 can be reduced to the form shown in Fig. 3 if we represent (for the sake of simplicity) the OFF-state FET impedance as a capacitor and the ON-state impedance as a resistor. If, by suitable design, the resistive components r_1 and r_2 are negligibly small compared with the resistive impedance in series or parallel with them, the circuit can be further simplified to the form shown in Fig. 4, which is a five-section low-pass filter.

In the opposite switch state, that is, when V_2 is equal to zero and V_1 is more negative than the device pinchoff voltage, the circuit of Fig. 2 reduces to the form shown in Fig. 5. If again, by suitable design, the resistive components r_3 and r_4 are small compared with the reactive impedances in series or parallel with them, the circuit can be further simplified to the form shown in Fig. 6. If the capacitors C_4 and C_5 are small enough that they do not shunt L_2 and L_3, this circuit has the basic form of a five-section high-pass filter.

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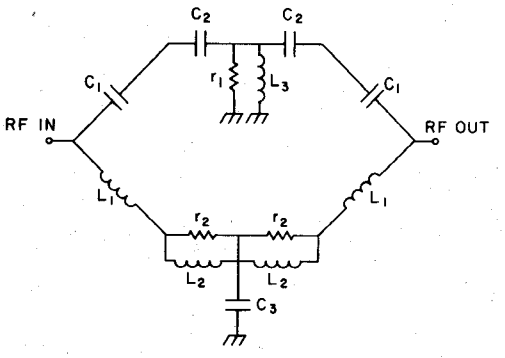

Fig. 3. The circuit shown in Fig. 2 where $V_1 = 0$ and $|V_2| > |V_p|$.

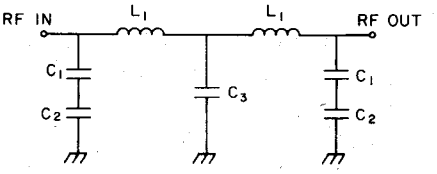

Fig. 4. The circuit shown in Fig. 3 reduces to this form if the resistive components r_1 and r_2 are small compared with the reactances in parallel with them.

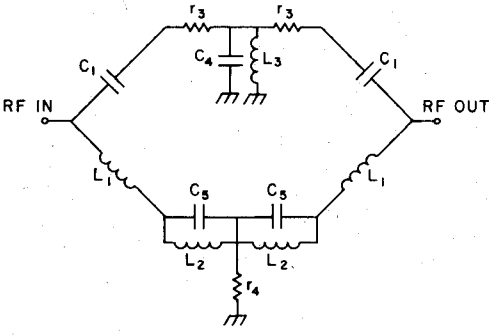

Fig. 5. The circuit shown in Fig. 2 when $|V_1| > |V_p|$ and $V_2 = 0$.

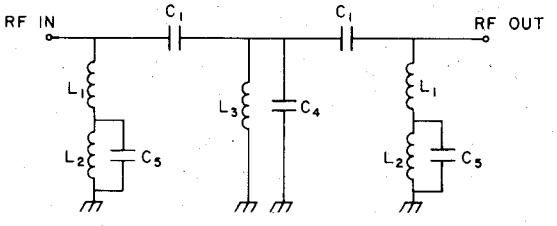

Fig. 6. The circuit shown in Fig. 5 reduces to this form if the resistive components r_3 and r_4 are small compared with the reactive impedances in series or parallel with them.

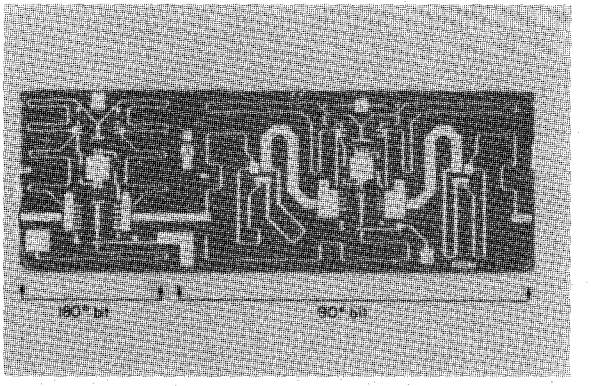

Fig. 7. Photograph of the finished chip.

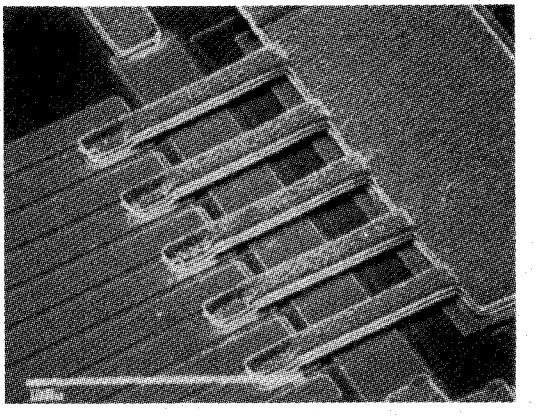

Fig. 8. SEM picture showing gate bias bus and the capacitor top plate-source finger overlay connection.

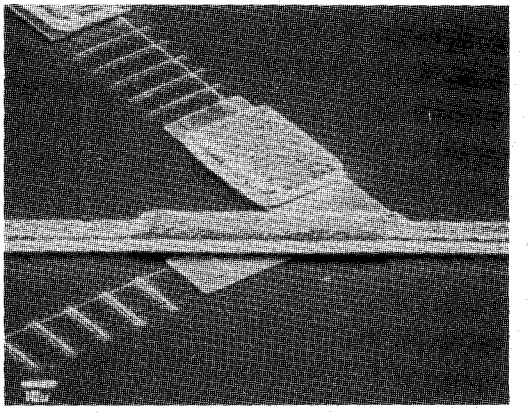

Fig. 9. SEM picture of a 10-μm-wide transmission line crossing over the gate bus with open-gate isolation resistors.

In summary, the bridge circuit shown schematically in Fig. 2 does allow us to realize a high-pass, low-pass phase shifter without external switch circuitry. Hence, the operating bandwidth can be maximized with a compact circuit layout.

This phase-shifter concept has been applied to a 2–8-GHz two-bit phase-shifter design. The inductors were realized using high-impedance transmission lines since large inductor values were not needed. Switching FET's are represented by their full model, including the effect of the gate control terminal [5]. During the design, both the periphery of the individual FET's and the input/output impedance levels were treated as parameters to be optimized. As the result of this optimization process, the periphery of the FET's in the circuit varies from as small as 83 μm to as large as 1333 μm. The 180° phase bit is designed for a 50-Ω system, whereas the 90° bit is designed for a 25-Ω system to improve VSWR. All the calculated and measured data presented in this paper include the effect of the impedance transformers required to bring the

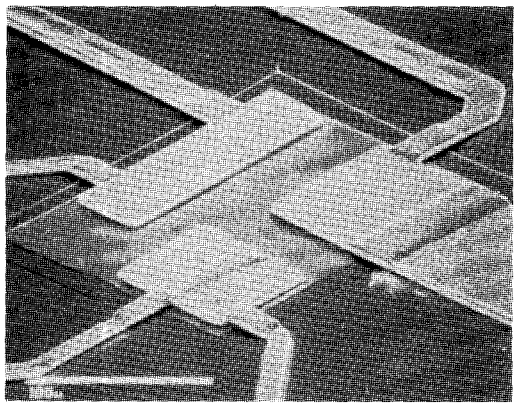

Fig. 10. Three capacitors sharing a single via hole pad as bottom plate. Top plates are connected through air bridges.

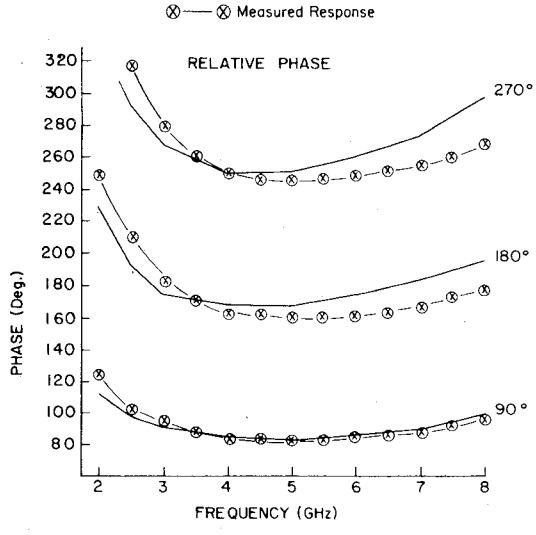

Fig. 11. Predicted and measured performance of the two-bit phase shifter.

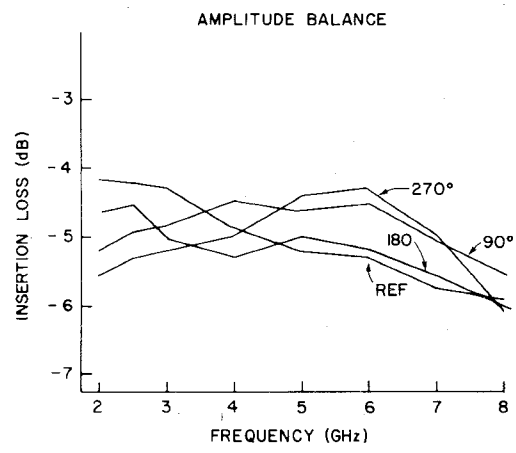

Fig. 12. Predicted insertion-loss performance of the phase shifter for each of the four phase shifters.

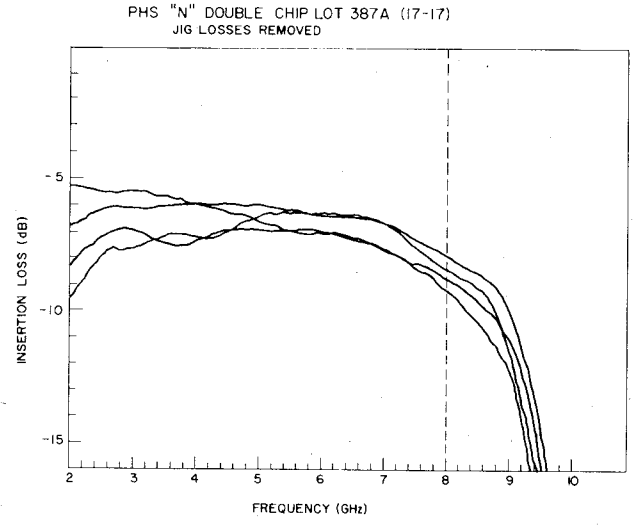

Fig. 13. Measured insertion-loss performance of the two-bit phase shifter for each phase state.

circuit to a 50-Ω system. The transformers are part of the monolithic circuit design.

III. Experimental Results

The two-bit phase shifter is designed and fabricated on 0.1-mm GaAs substrate in monolithic form. A photograph of the finished chip appears in Fig. 7. The chip dimensions are 4.8×1.7 mm (186×67 mils) with 7457 μm of total 0.9-μm gate periphery. Moving left to right on the chip, we see the the 180° bit 2:1 impedance transformer, the 90° bit, and the 1:2 impedance transformer.

The circuit configuration is fairly complex and requires several dc-RF crossovers. Fig. 8 shows how the top plate of a capacitor connects to the individual source fingers of an FET in series with it. Gates are connected to a metal strip which reaches to the gates of two other FET's on the opposite side. This gate bus also contains 2 kΩ open-gate resistors for RF isolation. These resistors are physically small and are intregrated into the bus. Fig. 9 shows a portion of this gate bus with the resistors passing under a 10-μm-wide RF transmission line. For size reduction, one via hole pad is shared among three thin-film capacitors as their bottom metal. Fig. 10 is a close-up view.

Fig. 11 shows the predicted and measured phase performance of the 2-bit design. Accounting for the shift in center frequency, the agreement is quite good. The measured insertion-loss performance for each phase state is shown in Figs. 12 and 13, respectively. The measured loss is 2–3 dB higher than predicted. This is primarily due to extra loss associated with the meander "horseshoe" sections used to conserve space (Fig. 7). The coupling in these sections was accounted for, but not the additional loss caused by the resultant asymmetrical field structure. The input/output return loss is better than 10 dB across the full frequency band.

The differential phase shift and insertion loss of individual 90° and 180° phase shifters are presented in Figs. 14 and 15, respectively. These figures compare several devices from three different lots with each other and with the theoretical prediction.

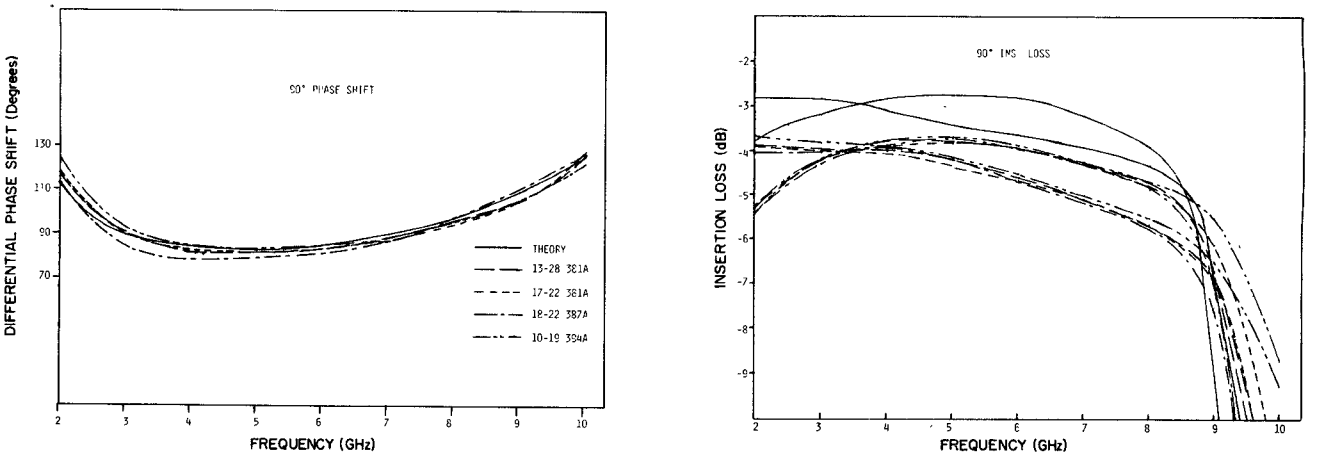

Fig. 14. Measured phase and insertion-loss date comparison for three different wafer lots: (a) differential phase, (b) insertion loss.

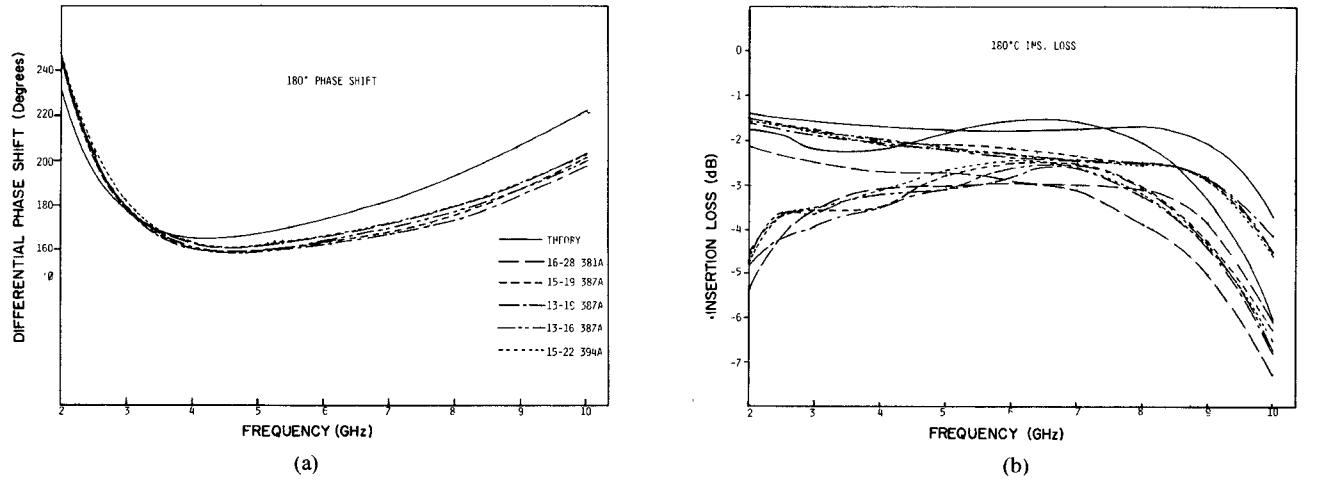

Fig. 15. Measured phase and insertion-loss comparison for three different wafer lots: (a) 180° bit phase shift, (b) 180° bit insertion loss.

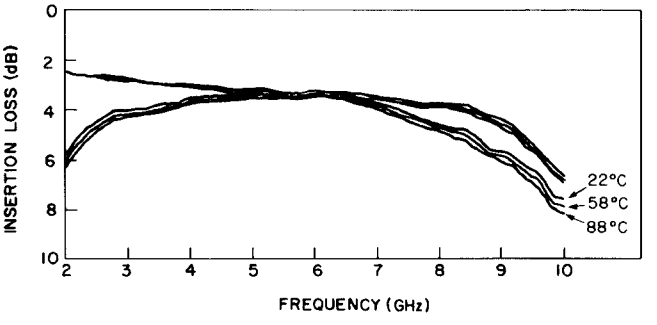

Fig. 16. Insertion loss of the two states at 22, 58, and 88°C.

The sensitivity to gate bias was checked by varying the gate voltage from −7 to −9 V. No change in phase or insertion loss was observed. This insensitivity to control signal is important because it guarantees that fluctuations in bias voltage as it switches back and forth between states will not translate into phase or amplitude noise.

Both phase and amplitude are also insensitive to temperature variations. Fig. 16 shows the insertion-loss data for a 180°C bit as the jig temperature is varied from 22 to 88°C. The differential phase shift varied less than 1° over this range.

The RF power-handling capability of the phase shifter was also investigated. Fig. 17 shows that, up to the 0.5-W level, no change in insertion loss is observed. Around the 1-W input power level, insertion loss increases by an additional 1 dB.

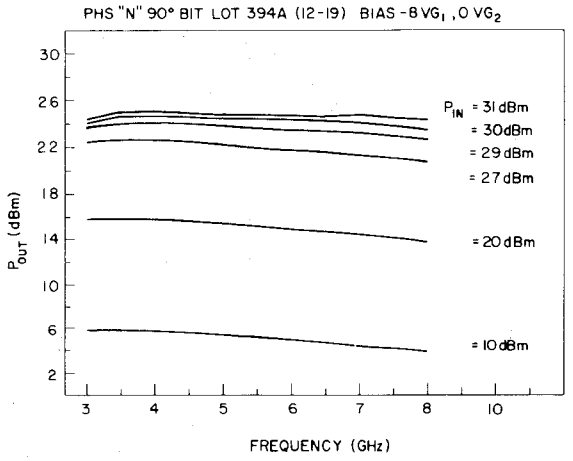

Fig. 17. Insertion loss of 90° bit phase bit at various input power levels.

IV. Conclusion

A novel approach, using nonideal switch elements as part of the phase-shifting low-pass or high-pass section, has been demonstrated in monolithic form using GaAs FET's as switch elements. This approach allows realization of the maximum theoretical bandwidth of an ideal high-pass/low-pass phase shifter. With a useable frequency bandwidth of 4:1, this phase shifter is an ideal component for use in phased arrays or broad-band signal processing.

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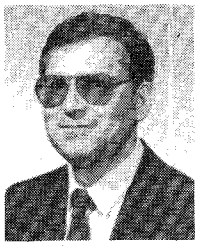

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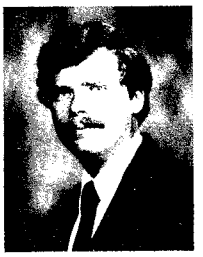

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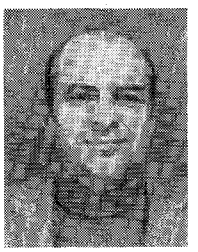

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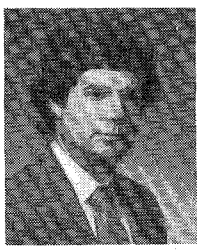
In December 1957, he joined the Raytheon Research Division where he has worked on ferrite structures, including cation distribution in spinels and other structural problems associated with ferrite materials. He developed improved techniques for studying thin films using total external reflection of X-rays. From 1963 to 1967, he attended the Massachusetts Institute of Technology, Cambridge, under a Raytheon advanced study grant. His studies at MIT culminated in a thesis on an X-ray diffraction study of the structure of glass. After returning to the Research Division in October 1967, he was responsible for the application of X-ray techniques, including X-ray topography, to the study of imperfections in single crystals. In addition to qualitative evaluations of the degree of perfection of a variety of single crystals and epitaxially grown thin films, he carried out more detailed studies of the structural damage induced by impurity diffusion in silicon and InSb crystals.



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